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10/733,953	12/10/2003	Ravi Kumar Arimilli	AUS920020194US1	8162

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EXAMINER	
RUIZ, ARACELIS	
ART UNIT	PAPER NUMBER
2189	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/733,953	ARIMILLI ET AL.	
	Examiner	Art Unit	
	ARACELIS RUIZ	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *12 September 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/8/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-18 are still present for examination.

Claims 1, 5, 6, 9 and 12-14 have been amended.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on August 8, 2006 is being considered by the examiner.

Specification

The disclosure is objected to because of the following informalities:

a. In page 1, paragraph 1, line 1, "U.S. Patent Application No. __/___,___" should be –U.S. Patent Application No. 10/733,948--..

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gharachorloo et al. (US Patent No. 6,697,919) in view of Lai et al. (US Publication no. 2003/0120881).

With respect to **claim 1**, Gharachorloo et al. teaches a data processing system (See FIG. 1), comprising: one or more processing cores (see column 4, lines 57-58, "...has eight processor cores"); and a memory controller, (see column 4, line 49, "...memory controller". See FIG. 1) coupled to said one or more processing cores (see column 4, lines 63-column 51 line 23; that each processor core has a memory controller. See also FIG. 1, element 118), that controls access to a system memory (see column 5, lines 4-7, "Memory controller (MC) 118 that preferably interfaces directly to a memory bank of DRAM (dynamic random access memory) chips...in a memory subsystem 123"), wherein said memory controller responsive to a memory access request (see FIG. 1, element 102), for speculatively (see FIGs. 4, 5, 7C, and 10C.; column 7, paragraphs 1-2) initiating access to the system memory (see column 11, line 19; "to advance memory transactions") based upon said historical information in said memory speculation mechanism (see column 8, lines 60-63, "...the directory entry is used by the home protocol engine (HPE) 122 to maintain cache coherence of the memory lines 184 corresponding to the directory entries 182.") in advance of receipt of a coherency message (see column 21, line 64, "protocol message") indicating that said memory access request is to be serviced by reference to said system memory (see column 22, paragraphs 1-2. Also see FIGs. 11A-14B).

With respect to **claim 2**, Gharachorloo et al. teaches wherein said memory controller and said one or more processing cores are integrated within a same integrated circuit chip (see column 2, lines 10-14, "...the Alpha 21364 aggressively exploits semiconductor technology trends by including a scaled 1 GHz 21264 core, two levels of caches, memory controller, coherence hardware, and network router all on a single die..." See FIG. 1).

With respect to **claims 3, 10 and 15**, Gharachorloo et al. teaches wherein said memory speculation mechanism comprises a memory speculation table ("directory", See rejection of claim 1 and FIGs. 4 and 10c) that stores a respective memory access history ("Directory Entry" of FIG. 4) for each of a plurality of threads executing within said one or more processing cores["simultaneous multithreading (SMT)" is disclosed in column 2, line 29. Also in column 1, lines 33-34, "instruction-level parallelism and speculative out-of-order execution" which teach this limitation).

With respect to **claims 4, 11 and 16**, Gharachorloo et al. teaches wherein said system memory (see FIG. 1, element 123) includes a plurality of storage locations (see abstract; "memory line") arranged in a plurality of banks (see column 5, lines 1-8; "each memory bank"), and wherein said memory speculation mechanism (see abstract; "directory") stores said historical information on a per-bank basis (see column 11, lines 56-61: "...the memory line address identifies the node 102, 104 that interfaces with the memory subsystem 123 that stores the memory line of information 184 (i.e., home node) and a specific position within the memory subsystem 123 of the memory line information." Also see FIG. 4, elements 180, 182, 184, 123).

With respect to **claims 5, 12 and 17**, Gharachorloo et al. teaches wherein said memory controller speculatively initiates access (See FIGs. 4, 5, 7C, and 10C; column 7, paragraphs 1-2) in advance of a combined response (see column 11, line 19, "to advance memory transactions") for said memory access request (see column 22, paragraphs 1-2. Also see FIGs. 11A-14B).

With respect to **claim 6**, Gharachorloo et al. teaches wherein said system memory comprises a first system memory (see column 4, lines 63-67 - column 5, lines 1-8, "memory bank"); said memory controller comprises a first memory controller (see column 4, lines 63-67 - column 5, lines 1-8, "memory controller"); said data processing system further comprising a second system memory and a second memory controller that controls access to the second system memory (see column 4, lines 63-67 - column 5, lines 1-8, that each (1st, 2nd, etc...) processor core has its own memory (L1 cache, L2 cache, memory bank of DRAM) as well as memory controller. See FIGs. 1 and 2); said memory controller speculatively initiates access to said first system memory based upon historical information recorded by said second memory controller (see column 21, lines 59-63, "The present invention includes a cache coherence protocol (CCP) that enables the sharing of memory lines of information 184 across multiple nodes 102, 104." Gharachorloo teaches that memory speculation can be accessed by another node (processor core, memory controller, etc.: element 102 of FIG. 1) through CCP. Also see limitation in rejection of claim 1 (also interpreted under 35 U.S.C. 112 6th paragraph) With respect to the limitation, "based upon historical information recorded by said second memory controller", the examiner notes that a second memory controller can be any of a plurality of memory controllers and therefore is interpreted as analogous to claim 1).

With respect to **claim 7**, Gharachorloo et al. teaches a system interconnect coupling said plurality of processing cores (see FIGs. 1-3, element 112, "lntra-chip switch (ICS)"); and one or more cache hierarchies coupled to said plurality of processing cores that cache data from said

system memory (see column 4, lines 63-67, "Each processor core (PC) 106 is directly connected to dedicated instruction cache (iLl) 108 and data cache (dL1) 110 modules. These first-level caches (L1 cache modules) 108, 110 interface to other modules through an intra-chip switch (ICS) 112").

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With respect to **claim 8**, Gharachorloo et al. teaches response logic that provides said combined response for said memory access request (see FIGs. 10C-14B).

With respect to **claims 9 and 14**, Gharachorloo et al. teaches a memory controller (see column 4, line 49; memory controller) for controlling access to a system memory (see FIG. 1, element 123; memory subsystem) of a data processing system (see FIG. 1), responsive to a memory access request (see FIG. 1, element 102) for speculatively (see FIGs. 4, 5, 7C, and 10C and column 7, paragraphs 1-2) initiating access to the system memory (see column 11, line 19, "to advance memory transactions") based upon said historical information in said memory speculation mechanism (see column 8, lines 60-63, "...the directory entry is used by the home protocol engine (HPE) 122 to maintain cache coherence of the memory lines 184 corresponding to the directory entries 182.) in advance of receipt of a coherency message (see column 21, line 64; protocol message) indicating that said memory access request is to be serviced by reference to said system memory (see column 22, paragraphs 1-2. Also see FIGs. 11A-14B).

With respect to **claims 13 and 18**, Gharachorloo et al. teaches wherein said control logic speculatively initiates access to said system memory based upon historical information recorded

by another memory controller (see column 21, lines 59-63, "The present invention includes a cache coherence protocol (CCP) that enables the sharing of memory lines of information 184 across multiple nodes 102, 104." Gharachorloo teaches that memory speculation can be accessed by another node (processor core, memory controller, etc.: element 102 of FIG. 1) through CCP).

Gharachorloo et al. does not teach said memory controller having a memory speculation mechanism that stores historical information regarding whether prior memory accesses were serviced by accessing the system memory as recited in claim 1; a memory speculation mechanism that stores historical information regarding whether prior memory accesses were serviced by accessing said system memory as recited in claim 9; and said memory controller storing in a memory speculation mechanism historical information regarding whether prior memory accesses were serviced by access to the system memory as recited in claim 14. Lai et al. teaches a table that track the history of previous operations to a memory unit (see page 2, paragraph 29, lines 1-5). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the method taught by Gharachorloo et al. to include the above mentioned because it can help to increase the rate of page hit to a memory unit (see page 2, paragraph 29, lines 5-11).

Response to Arguments

Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection, necessitated by amendment.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ARACELIS RUIZ whose telephone number is (571)270-1038. The examiner can normally be reached on Monday-Thursday 7:30-6:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aracelis Ruiz/
Examiner, Art Unit 2189

/Reginald G. Bragdon/
Supervisory Patent Examiner, Art Unit 2189